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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,790	01/23/2004	Pengfei Zhang		6143

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EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/762,790	ZHANG ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☒ Claim(s) *2-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/762,790 filed on 01/23/2004. Claims 1 – 11 remain pending in the application.

Claim Objections

2. Claims listed below are objected to because of the following informalities:

Claim 1, line 2, before "partitioning" delete —**and**—.
Claim 1, line 4, before "software program" insert —**a**—.
Claim 2, line 2, change "Providing a memory ...said memory; and" to —**providing a series of rules;**—.
Claim 2, line 2, change "Storing said series of rule in said memory; and" to —**storing said series of rule in a first memory;**—.
Claim 2, line 4, change "Providing a memory that is able to store" to —**providing**—.
Claim 2, line 6, delete —**and**—.
Claim 2, line 7, change "Storing said circuit netlist in said memories; and" to —**storing said circuit netlist in a second memory;**—.
Claim 2, after line 7, insert —**(e) storing signal flow information in a third memory; and**—.
Claim 2, line 8, change "(e) Utilizing" to —**(f) utilizing**—.
Claim 2, line 8, before "signal flow information" insert —**said**—.
Claim 2, line 9, change "netlist; and" to —**netlist.**—.
Claim 2, line 10, delete —**(f) Storing said signal flow...in said memory.**—.
Claim 3, line 2, before "partition" to —**signal flow driven circuit**—.
Claim 3, line 3, change "(a) Utilizing the signal flow...claim 2 wherein" to —**(a) utilizing**—.
Claim 3, line 4, delete —**claim 2**—.
Claim 3, line 5, delete —**and**—.
Claim 3, line 6, change "Providing a memory that is able to store" to —**providing**—.
Claim 3, line 7, delete —**and**—.

Claim 3, line 8, change "Storing said series of critical signal flow requirements in said memory; and" to **—storing said series of critical signal flow requirement in a fourth memory;—**.
Claim 3, line 9, change "Utilizing" to **—utilizing—**.
Claim 3, line 11, delete **—and—**.
Claim 3, line 12, change "Utilizing" to **—utilizing—**.
Claim 3, line 14, before "unit circuit of circuit reference" insert **—an—**.
Claim 3, line 15, delete **—and—**.
Claim 3, line 16, change "Utilizing" to **—utilizing—**.
Claim 3, line 16 – 17 (3 places), delete **—multitude—**.
Claim 3, line 18, delete **—of claim2—**.
Claim 3, line 19, change "Providing a memory that is able to store" to **—providing a fifth memory for storing—**.
Claim 3, line 20, line 20, change "component; and" to **—component.—**.
Claim 3, line 21 – 22, delete **—(h) Storing said critical nodes...in said memory.—**.
Claim 4, line 1, change "claim 1" to **—claim 3—**.
Claim 4, line 3, change "(a) Providing a memory that is able to store" to **—(a) providing—**.
Claim 4, line 4, delete **—and—**.
Claim 4, line 5, change "Storing said series of physical requirement rule in said memory; and" to **—storing said series of physical requirement rules in a sixth memory;—**.
Claim 4, line 6, change "Utilizing the signal flow driven circuit analysis technique of claim 2 wherein" to **—utilizing—**.
Claim 4, line 7 – 8, change "and the signal flow driven circuit partition technique of claim 3 wherein" to **—said series of critical signal flow requirements of the signal flow driven circuit partition technique for identifying—**.
Claim 4, line 9, before "physical requirement rules" insert **—series of—**.
Claim 4, line 11, change "loading; and" to **—loading thereby being able to layout an analog circuit, a mixed signal circuit, and a RF circuit automatically by an engineer.—**.
Claim 4, line 12 – 13, delete **—Whereby an engineer...a RF circuit automatically.—**.

Claim 5, line 1, change "A mean of circuit performance assessment utilizing:" to –**–The signal flow driven circuit analysis technique of claim 4 further being implemented in a means of circuit performance assessment utilizing:—**.
Claim 5, line 2 – 3, change "The signal flow driven circuit analysis technique of claim 2 wherein said signal flow information; and" to **—said signal flow information of the signal flow driven circuit analysis technique;—**.
Claim 5, line 4 – 5, change "The signal flow driven circuit partition technique of claim 3 wherein" to **—said serial of critical signal flow requirements of the signal flow driven circuit partition technique for identifying—**.
Claim 5, line 6 – 7, change "The physical layout constraint generation technique of claim 4 wherein said physical requirement rules" to **—said serial of physical requirement rules of the physical layout constraint generation technique—**.
Claim 6, line 1, change "A mean of circuit yield enhancement utilizing:" to **—The signal flow driven circuit analysis technique of claim 4 further being implemented in a means of circuit yield enhancement utilizing:—**.
Claim 6, line 2 – 3, change "The signal flow driven circuit analysis technique of claim 2 wherein said signal flow information; and" to **—said signal flow information of the signal flow driven circuit analysis technique;—**.
Claim 6, line 4 – 5, change "The signal flow driven circuit partition technique of claim 3 wherein" to **—said serial of critical signal flow requirements of the signal flow driven circuit partition technique for identifying—**.
Claim 6, line 6 – 7, change "The physical layout constraint generation technique of claim 4 wherein said physical requirement rules" to **—said serial of physical requirement rules of the physical layout constraint generation technique—**.
Claim 7, line 1, change "A circuit hierarchy regeneration technique comprising:" to **—The signal flow driven circuit analysis technique of claim 4 further being implemented in a circuit hierarchy generation technique comprising:—**.
Claim 7, line 2 – 3, change "The signal flow driven circuit analysis technique of claim 2 wherein said signal flow information; and" to **—said signal flow information of the signal flow driven circuit analysis technique;—**.
Claim 7, line 4 – 5, change "The signal flow driven circuit partition technique of claim 3 wherein" to **—said serial of critical signal flow requirements of the signal flow driven circuit partition technique for partitioning—**.

Claim 7, line 7 – 8, change "The physical layout constraint generation technique of claim 4 wherein said circuit physical layout constraints of" to **—said multitude circuit physical layout constraints of the physical layout constraint generation technique for—**.

Claim 7, line 11, change "loading; and" to **—loading thereby improving an analog circuit, mixed signal circuit, and RF circuit simulation speed by an engineer.—**.

Claim 7, line 10 – 11, delete **—Whereby an engineer...a RF circuit simulation speed.—**.

Claim 8, line 1, change "A circuit performance optimization technique utilizing:" to **—The signal flow driven circuit analysis technique of claim 4 further being implemented in a circuit performance optimization technique utilizing:—**.

Claim 8, line 2 – 3, change "The signal flow driven circuit analysis technique of claim 2 wherein said signal flow information; and" to **—said signal flow information of the signal flow driven circuit analysis technique;—**.

Claim 8, line 4 – 5, change "The signal flow driven circuit partition technique of claim 3 wherein" to **—said serial of critical signal flow requirements of the signal flow driven circuit partition technique for partitioning—**.

Claim 8, line 7 – 8, change "The physical layout constraint generation technique of claim 4 wherein said circuit physical layout constraints of" to **—said multitude circuit physical layout constraints of the physical layout constraint generation technique for—**.

Claim 9, line 1, change "A circuit physical layout optimization technique utilizing:" to **—The signal flow driven circuit analysis technique of claim 4 further being implemented in a circuit physical layout optimization technique utilizing:—**.

Claim 9, line 2 – 3, change "The signal flow driven circuit analysis technique of claim 2 wherein said signal flow information; and" to **—said signal flow information of the signal flow driven circuit analysis technique;—**.

Claim 9, line 4 – 5, change "The signal flow driven circuit partition technique of claim 3 wherein" to **—said serial of critical signal flow requirements of the signal flow driven circuit partition technique for partitioning—**.

Claim 9, line 7 – 8, change "The physical layout constraint generation technique of claim 4 wherein said circuit physical layout constraints of" to **—said multitude**

circuit physical layout constraints of the physical layout constraint generation technique for—.

Claim 10, line 1, change "A circuit physical layout floor planning utilizing:" to —**The signal flow driven circuit analysis technique of claim 4 further being implemented in a circuit physical layout floor planning utilizing:—.**

Claim 10, line 2 – 3, change "The signal flow driven circuit analysis technique of claim 2 wherein said signal flow information; and" to —**said signal flow information of the signal flow driven circuit analysis technique;—.**

Claim 10, line 4 – 5, change "The signal flow driven circuit partition technique of claim 3 wherein" to —**said serial of critical signal flow requirements of the signal flow driven circuit partition technique for partitioning—.**

Claim 10, line 7 – 8, change "The physical layout constraint generation technique of claim 4 wherein said circuit physical layout constraints of" to —**said multitude circuit physical layout constraints of the physical layout constraint generation technique for—.**

Claim 11, line 1, change "A mean of extracting Intellectual Property circuit cell utilizing:" to —**The signal flow driven circuit analysis technique of claim 4 further being implemented in a means of extracting intellectual Property circuit cell utilizing:—.**

Claim 11, line 2 – 3, change "The signal flow driven circuit analysis technique of claim 2 wherein said signal flow information; and" to —**said signal flow information of the signal flow driven circuit analysis technique;—.**

Claim 11, line 4 – 5, change "The signal flow driven circuit partition technique of claim 3 wherein" to —**said serial of critical signal flow requirements of the signal flow driven circuit partition technique for partitioning—.**

Claim 11, line 7 – 8, change "The physical layout constraint generation technique of claim 4 wherein said circuit physical layout constraints of" to —**said multitude circuit physical layout constraints of the physical layout constraint generation technique for—.**

Appropriate corrections are required.

Claim Objections

3. The disclosure of Claims 2 – 11 is objected to under 37 CFR 1.71, as being so incomprehensible as to preclude a reasonable search of the prior art by the examiner.

For example, in Claim 2, applicants cite "*Providing **a memory** that is able to store a circuit netlist*" in line 4, and "*Storing said circuit netlist in said **memories***" in line 7. It is not clear how many memories and which memory will be used in storing a circuit netlist.

Applicant is required to submit an amendment, which clarifies the disclosure so that the examiner may make a proper comparison of the invention with the prior art.

Applicant should be careful not to introduce any new matter into the disclosure (i.e., matter which is not supported by the disclosure as originally filed).

Claim 2 cited above is objected. Claims 3 – 11 are also objected because of the cited deficiencies of Claim 2 on which they dependent upon.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being unpatentable over U.S. Patent No. 5,740,347 to *Avidan*.

6. As to Claim 1, *Avidan* shows and teaches the following subject matter:

- Circuit analyzer using enhanced rule-based circuit analysis technique by (tracing) signal flow direction in a circuit in setting algorithm to analyze a circuit, to partition a circuit and to generate multitude circuit layout constraints – [title; abstract; col. 8, line 60 – col. 9, line 63; col. 1, line 15 – 34; Figs. 26A – 26C]; Notice that circuit analyzer using embedded software program to perform enhanced rule-based circuit analysis technique automatically.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Patent Examiner
Art Unit 2825
December 7, 2005